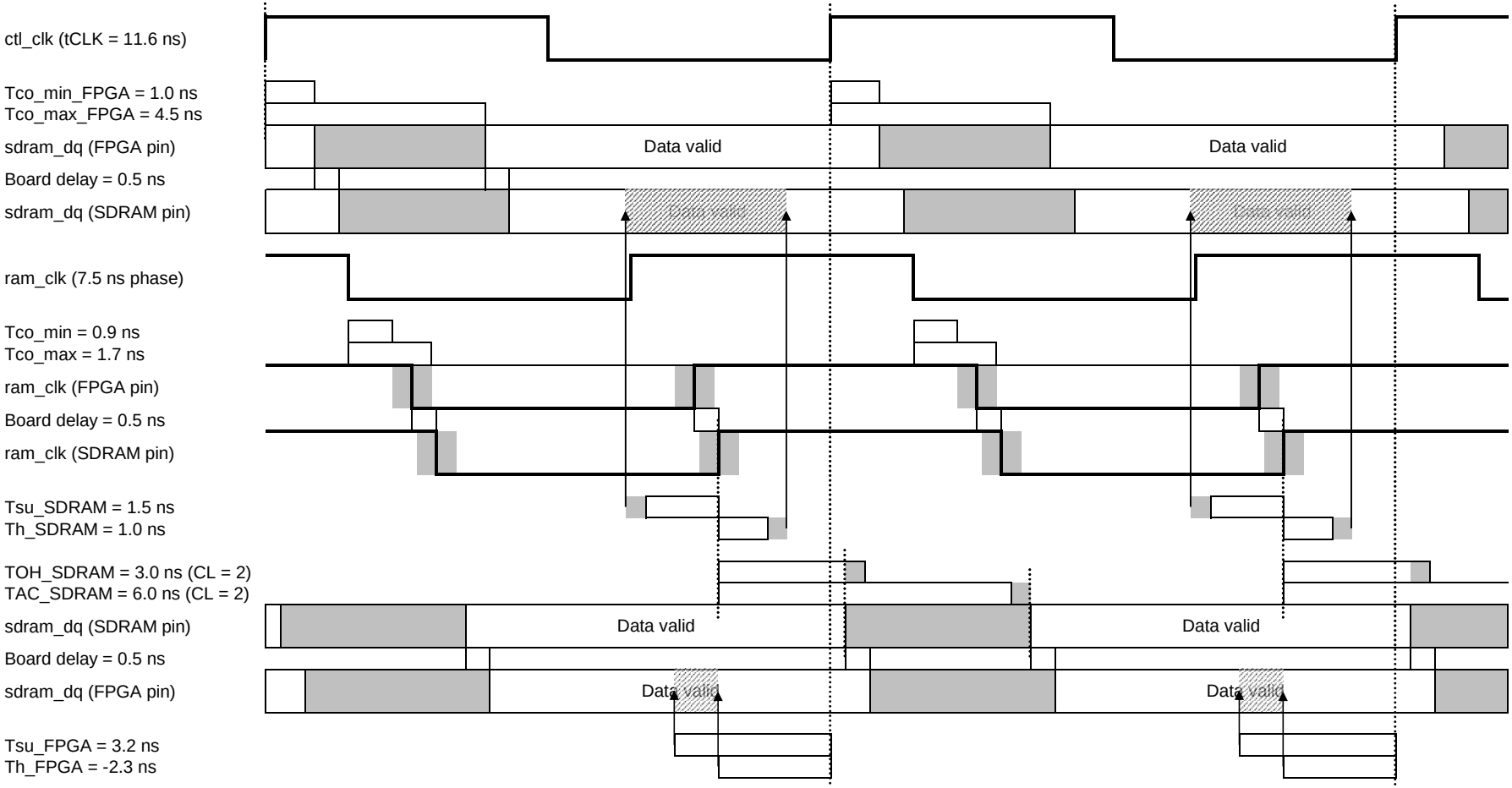
ctl_clk (tCLK = 11.6 ns)
Tco_min_FPGA = 1.0 ns
Tco_max_FPGA = 4.5 ns
sdram_dq (FPGA pin)
Data valid
Data valid
Board delay = 0.5 ns
sdram_dq (SDRAM pin)
Data valid
Data valid
ram_clk (7.5 ns phase)
Tco_min = 0.9 ns
Tco_max = 1.7 ns
ram_clk (FPGA pin)
Board delay = 0.5 ns
ram_clk (SDRAM pin)
Tsu_SDRAM = 1.5 ns
Th_SDRAM = 1.0 ns
TOH_SDRAM = 3.0 ns (CL = 2)
TAC_SDRAM = 6.0 ns (CL = 2)
sdram_dq (SDRAM pin)
Data valid
Data valid
Board delay = 0.5 ns
sdram_dq (FPGA pin)
Data valid
Data valid
Tsu_FPGA = 3.2 ns
Th_FPGA = -2.3 ns