TRIPLE-PORT DRAM

256K x 4 DRAM WITH DUAL 512 x 4 SAMS

FEATURES

- Three asynchronous, independent, data-access ports
- Fast access times: 80ns random, 25ns serial
- Operation and control compatible with 1 Meg VRAM
- High-performance, CMOS silicon-gate process
- Inputs and outputs are fully TTL compatible
- Low power: 15mW standby; 500mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- FAST-PAGE-MODE access cycles
- Two bidirectional serial access memories (SAMs)
- Fully static SAM and Mask Register, no refresh required
- 2,048-bit Bit Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

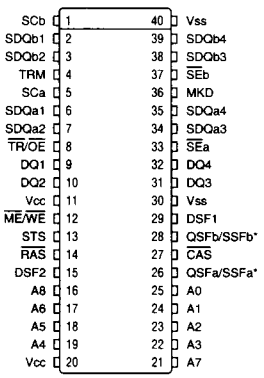
- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ and WRITE TRANSFERs
- BLOCK WRITE
- BIT MASKED TRANSFERs

OPTIONS — MARKING

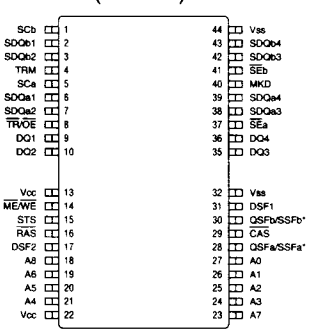
- Timing (DRAM, SAMs [cycle/access])
  - 80ns, 28ns/25ns — - 8
  - 100ns, 30ns/27ns — -10
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- Functionality
  - QSF output (indicates SAM-half accessed) — MT43C4257
  - SSF input (Split SAM special function, stop count) — MT43C4258
- Part Number Example: MT43C4257DJ-8

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(SDB-3)



40/44-Pin TSOP**
(SDE-2)



*MT43C4257/MT43C4258
**Consult factory for TSOP availability.

GENERAL DESCRIPTION

The MT43C4257/8 are high-speed, triple-port CMOS dynamic random access memories (TPDRAMs) containing 1,048,576 bits. Data may be accessed by a 4-bit-wide DRAM port or by either of two independently clocked 512 x 4-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and either SAM.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Eight 512-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 4-bit random access I/O port, the pair of internal 2,048-bit-

wide paths between the DRAM and the SAMs, and the pair of 4-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing and address decoding logic.

All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2,048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 512 x 4-bit bit mask data register can be parallel loaded from the DRAM or either SAM, or serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of $\overline{RAS}$ addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require refresh.

The operation and control of the MT43C4257/8 are optimized for high performance graphics and communication designs. The triple-port architecture is well suited to buffering the sequential data types used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER, BIT MASKED TRANSFERs and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM