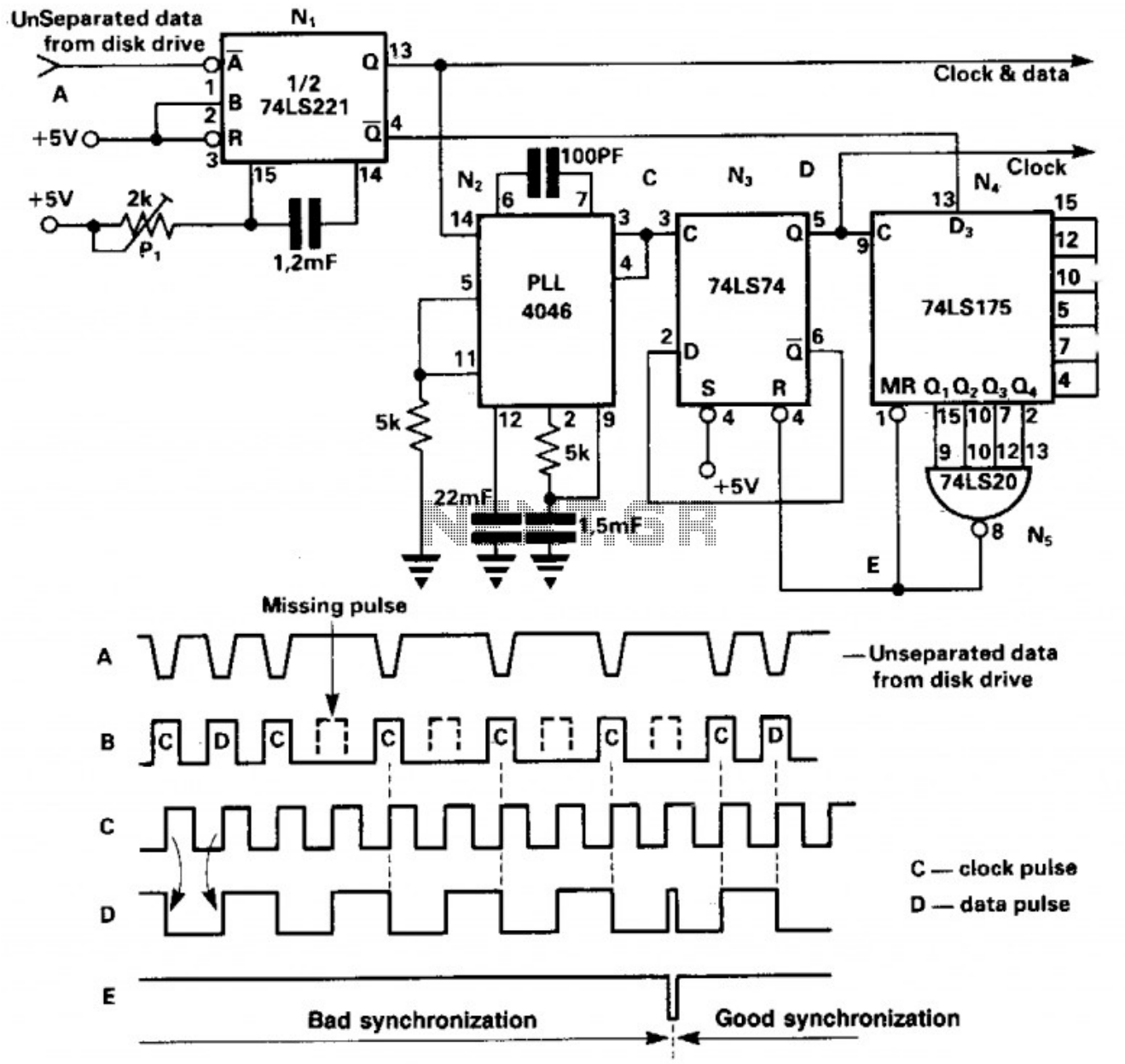

The data separator is intended for use with 8` flexible diskettes with IBM 3870 soft sectored format. The circuit delivers data and clock (B) and clock pulses (D). These two signals must be in such a sequence that the negative edge of the clock pulse is at the middle of a data cell. Unseparated data (A) from the floppy unit is shaped with one shot Nl. Trimmer PI should be adjusted so that pulses (B) are 1 ?& wide.

This signal synchronizes PLL N2 with a free running frequency adjusted to 500 kHz. The output of the PLL is 90Â° out of phase with its input. D-type flip-flop N3 is connected as a divider by two and changes state at each positive edge of (C). N4, connected as a shift register, looks for four consecutive missing pulses. When this happens, the circuit is resynchronized with (E) so that the negative edge of (D) is in the middle of a data cell.